REMARKS

Applicant respectfully requests the reconsideration of this application and the consideration of the following remarks.

Claims 11-24 and 35-48 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,397,324 (hereinafter "Barry"). Applicant respectfully disagrees.

Applicant respectfully submits that Barry does not show each and every aspect of claims 11 and 35 and their dependent claims.

For example, claim 11 recites:

> 11. (Original) A method for execution by a microprocessor in response to receiving a single instruction, the method comprising:
> receiving a plurality of numbers;
> partitioning look-up memory into a plurality of look-up tables;
> looking up simultaneously a plurality of elements from the plurality of look-up tables, each of the plurality of elements being in one of the plurality of look-up tables and being pointed to by one of the plurality of numbers;
> wherein the above operations are performed in response to the microprocessor receiving the single instruction.

Applicant respectfully submits that Barry (Col., 10, lines 24-45; Col. 10, line 62 to Col. 11, lines 48; and Col. 11, line 65 to Col. 12, line 27) does not show "partitioning look-up memory into a plurality of look-up tables" "in response to the microprocessor receiving the single instruction".

The Office Action asserted that Barry (Col., 10, lines 24-45; Col. 10, line 62 to Col. 11, lines 48; and Col. 11, line 65 to Col. 12, line 27) describes

"how the memory is separated into multiple "imaginary" banks, i.e., partitioned into look-up memory, that holds the data for a particular table, i.e., a particular table from a plurality of tables". (Item 57, page 17, Office Action mailed February 9, 2005).

However, from the description of Barry (Col., 10, lines 24-45; Col. 10, line 62 to Col. 11, lines 48; and Col. 11, line 65 to Col. 12, line 27), it is apparent that separating memory into separate banks is a design choice, which is a decision made by a human being but not an operation performed by the processor in response to receiving an instruction.

For example, Col. 11, lines 33-38, of Barry shows

"Quad Address Table Look-Up (L4TBL) To support this instruction type, the SP and each PE data memories are split into four separate banks which are addressable independently. The addressing mechanism is organized in a similar manner to the dual table apparatus with extensions to support four banks of memory bank-0 to bank-3." (Col. 11, lines 33-38, Barry)

Thus, it is understood that the SP and each PE data memories of Barry are ***split***, by design, into four separate banks, bank-0 to bank-3, to support the L4TBL instruction. According to the description of Barry (e.g., Col. 11, lines 9-10), bank-0 and bank-1 are used to support the L2TBL instruction. Thus, if the processor by design has only two independently addressable banks, bank-0 and bank-1, the L4TBL instruction is not supported. To support the L4TBL instruction, the processor is to be designed to have four independently addressable banks, bank-0 to bank-3. Thus, it is clear that, to design the processor according to Barry, a human being arranges to split the data memories into separate banks that are independently addressable. The processor of Barry cannot and does not split the memories into separate, independently addressable banks in response to either the L2TBL instruction or the L4TBL

instruction of Barry. Therefore, Barry does not show "partitioning look-up memory into a plurality of look-up tables" "in response to the microprocessor receiving the single instruction".

Applicant respectfully submits that an ordinary person understood that a human being is not a microprocessor. What a human being performs to design a processor cannot be considered as what the processor performs in response to a single instruction. Thus, Barry does not show each and every aspect of claim 11. The withdrawal of the rejection under 35 U.S.C. 102(e) for claim 11 is respectfully requested.

Claims 12-24 depend from claim 11 to incorporate the limitations of claim 11. Claims 35-48 recite similar limitations as discussed above. Thus, at least for the above reasons, Barry does not show each and every aspect of claims 11-24 and claims 35-48.

Claims 1-10, 25-34 and 49-50 were rejected under 35 U.S.C. 103(a) as being unpatentable over Barry in view of U.S. Patent No. 5,768,628 (hereinafter "Priem"). Applicant respectfully disagrees. Applicant respectfully submits that when the cited references are view as a whole, the subject matter as recited in the pending claims is not obvious.

Applicant respectfully submits that there is no indication in Barry and Priem that would lead to the particular arrangements recited in claims 1-10, 25-34 and 49-50.

Claim 1, for example, recites:

> 1. (Previously Presented) A method for execution by a microprocessor in response to receiving a single instruction, the method comprising:
> receiving a first plurality of numbers and a second plurality of numbers, each of the first plurality of numbers pointing to one of a plurality of entries, each of the plurality of entries being in one of a plurality of look-up tables; and

replacing simultaneously the plurality of entries in the plurality of look-up tables with the second plurality of numbers;

wherein the above operations are performed in response to the microprocessor receiving the single instruction;

wherein the microprocessor is a media processor integrated with a memory controller for host memory on a single integrated circuit.

The Office Action asserted that

> "Priem has taught wherein the microprocessor comprises a media processor integrated with a memory controller for host memory on a single integrated circuit (Priem Abstract; column 6, lines 45 to column 7, lines 35; column 7, line 56 to column 8, line 4; Figure 3; and Figure 4)." (Item 38, page 9, Office Action mailed February 9, 2005).

Applicant respectfully disagrees.

Figure 3 of Priem shows a sound card (51). A person skilled in the art understood that a sound card is a circuit board, not a media processor on an integrated circuit chip. The description of a sound card should not be construed as a description for a media processor. Thus, this assertion of the Office Action is erroneous.

Further, even if Barry and Priem were combined, the DMA would be on a circuit board (e.g., a sound card), separate from the processor of Barry. Thus, the combination would not show each and every aspect of claim 1.

Further, the disclosure of Barry shows that Barry et al. were aware of the use of DMA. For example, Barry explicitly shows the DMA (see, e.g., Figure 1, DMA 181 of Barry) in the system of Barry. It is apparent that Barry et al. understood the use of DMA. Barry explicitly mentioned DMA but designed the system in a way different from what is

claimed. Thus, the fact that Barry failed to describe the subject matter as claimed provides the clear indication of non-obviousness.

It does not appear that the description of Priem would inspire Barry et al. further toward the subject matter as claimed, since Barry et al. were aware of the use of DMA. Furthermore, Barry was filed in 2000 which was many years after Priem was filed in 1995 and issued in 1998. Thus, applicant respectfully submits the modification suggested in the Office Action was based on the hindsight afforded by the teaching of the present invention.

Note that claim 1 recite "the microprocessor is a media processor integrated with a memory controller for host memory on ***a single integrated circuit***". A sound card is not a single integrated circuit. Claim 23 recites similar limitations as claim 1. Thus, when viewed together, Barry and Priem do not include all the limitations as recited in claims 1 and 23 and their dependent claims.

Claims 4 and 5, for example, recite:

4. (Original) A method for execution by a microprocessor in response to receiving a single instruction, the method comprising:
replacing at least one entry in at least one of a plurality of look-up units in a microprocessor unit with at least one number using a Direct Memory Access (DMA) controller;
wherein the above operations are performed in response to the microprocessor receiving the single instruction.

5. (Original) A method for execution by a microprocessor in response to receiving a single instruction, the method comprising:
replacing at least one entry for each of a plurality of look-up units in a microprocessor with a plurality of numbers using a Direct Memory Access (DMA) controller;

wherein the above operations are performed in response to the microprocessor receiving the single instruction.

The Office Action asserted that

> "A person of ordinary skill in the art at the time the invention was made would have recognized that the memory controller allows data transfers to occur as quickly as possible (Priem column 6, lines 52-54), thereby increasing processor speed and efficiency (Priem column 2, line 64 to column 3, line 5)."

Applicant respectfully assumes that the Office Action intended to cite the advantages of using DMA as described in Priem, not just using any memory controller.

Applicant respectfully request the examiner consider the fact that Barry actually describes the used of a DMA but fail to present the subject matter as claimed. Priem was filed in 1995 and issued in 1998, years before Barry was filed in 2000. Barry et al. would be considered as persons skilled in the art. However, Barry et al. failed to design an instruction as recited in claim 4 or claim 5, even though Barry et al. appeared to have the knowledge about DMA (see, e.g., Figure 1, DMA 181) in general. This fact is a clear indication of non-obviousness. The description of Priem would inspire Barry et al. further toward the subject matter as claimed. Thus, applicant respectfully submits that the specific arrangements as recited in claims 4 and 5 were not obvious in view of Barry and Priem.

Claims 28 and 29 recite similar limitations as discussed above.

Further, the description of Priem is about a sound card, which is not a processor. Using the elements of Priem about a sound card to fill in the gaps between the instruction of Barry and the claimed subject matter of the present application (e.g., for claims 4, 5, 28, 29 and their dependent claims) appears to be a hindsight reconstruction, which is impermissible.

The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness under 35 U.S.C. 103. A prima facie case of obviousness is established by presenting evidence that would have led one of ordinary skill in the art to combine the relevant teachings of the references to arrive at the claimed invention. **It is impermissible to simply make a hindsight reconstruction of the claimed invention using the claim as a template and filling the gaps using the elements from the references.**

"The tendency to resort to hindsight upon applicant's disclosure is often difficult to avoid due to the very nature of the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art." (MPEP 2142).

MPEP (2141) shows that "When applying 35 U.S.C. 103, the following tenets of patent law must be adhered to: (A) The claimed invention must be considered as a whole; (B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; (C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and (D) Reasonable expectation of success is the standard with which obviousness is determined."

Further, MPEP (2142, 2143) shows that "To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure."

A broad conclusory statement regarding the obviousness of modifying a reference, standing along, is not "evidence".

Thus, the withdrawal of the rejections under 35 U.S.C. 103(a) is respectfully requested.

Please charge any shortages or credit any overages to Deposit Account No. 02-2666. Furthermore, if an extension is required, Applicant hereby requests such extension.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 8/10, 2005

Lehua Wang
Reg. No. 48,023

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025-1026
(408) 720-8300